EC2254 - LINEAR INTEGRATED CIRCUITS

Time: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. What is an integrated circuit?
2. What is current mirror?
3. Give the schematic of op-arnp based current to voltage converter.
4. Draw the circuit diagram of differentiator and give its output equation.
5. What is a VCO?
6. Draw the relation between the capture ranges and lock range in a PLL.
7. Define resolution of a data converter.
8. Give the advantages of integrating type ADC.
9. Draw the internal circuit for audio power amplifier.
10. What are the three different wave forms generated by ICL8038?

PART B - (5 x 16 = 80 Marks)

11. (a) (i) Define CMRR. Draw the circuit of an Op-arnp differential amplifier and give the expression for CMRR. (8)

(ii) Define Slew Rate. Explain the cause of slew rate and derive an expression for Slew rate for an op-arnp voltage follower. (8)

Or

(b) Briefly explain the various processes involved in fabricating monolithic IC which integrates bipolar transistor, diode, capacitor and resistor. (16)

12. (a) (i) Design a first order Low-pass filter for cut-off frequency of 2 KHz and pass-band gain of 2. (8)

(ii) Explain a positive clipper circuit using an Op-amp and a diode with neat diagrams. (8)

Or

(b) (i) Design a circuit to implement $Va = O.545V_3 + O.273V_4 - 1.25V_j - 2V_2$. (8)

(ii) Draw and explain a simple Op-amp differentiator. Mention its limitations. Explain with a neat diagram how it can be overcome in a practical differentiator. Design an Op-arnp differentiator that will differentiate an input signal with maximum frequency $f_{max} = 100Hz$. (8)

13. (a) (i) With a neat diagram explain the variable transconductance technique in analog multiplier and give its output equation. (8)

(ii) Briefly explain the working of voltage controlled oscillator. (8)

Or

(b) What are important building block of phase locked loop (PLL) explain its Working? (16)

14. (a) (i) Explain the working of R-2R ladder DAC. (8)

(ii) Explain the working of success approximation ADC. (8)

Or

(b) (i) A dual slope ABC uses a 16-bit counter and a 4 MHz clock rate. The maximum input voltage is +10V. The maximum integrator output voltage should be -8V when the counter has recycled through 2^n counts. The capacitor used in the integrator is $O.l,uF$. Find the value ofresistor R of the integrator. (8)

(ii) vVhat is a sample and hold circuit? Briefly explain its construction and application. (8)

15. (a) (i) How is voltage regulators classified? Explain a series voltage regulator. (8)

(ii) What is an optocoupler? Briefly explain its characteristics. (8)

Or

(b) With a neat circuit diagram and internal functional diagram explain the working of 555 timers in astable mode. (16)